NextDrive® IVCR1412 Compact SiC MOSFET Driver with Integrated Negative Bias and Miller Effect Suppression

1. Features

- 6-pin SOT-23
- Up to 2A peak source and 4A sink drive current
- 80ns sink current fold back control
- Wide VDD range up to 30V
- VDD operation from 4.5V to 25V with UVLO protection
- Integrated -2V negative voltage output(default) with 0V negative bias option
- Miller Effect suppression
- Configurable output driving current
- Ability to handle negative (-5V) input
- TTL and CMOS compatible input
- Low propagation delay (16ns)
- Output held low when floating input
- Operating temperature range -40°C to 125°C

2. Applications

- Emerging Wide Band-Gap power devices
- Paralleled power devices' drive
- Motor drives
- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- EV/HEV inverters and DC/DC converters
- PV boosters and inverters
- UPS

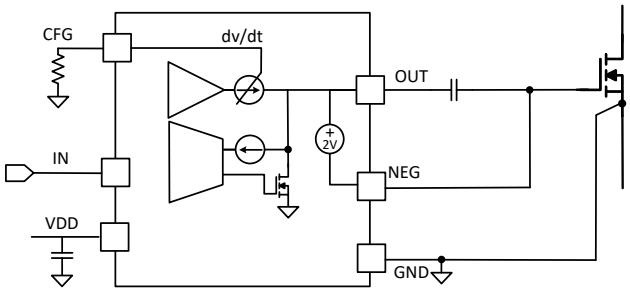
3. Description

IVCR1412 is one of NextDrive® family products. It is a compact driver, which has only 6 pins and uses SOT-23 package. The driver's output is driven by a current source, which eliminates all gate resistors and minimizes gate drive loop stray inductance. The driver integrates a negative voltage charge pump to provide a -2V turn-off voltage. OUT can be used directly if -2V is not needed. Due to no gate resistors existing at the gate drive loop, a strong pull-down control at the driver's output pin can serve as an active Miller effect suppression function and turn off a MOSFET reliably. At turn off, the driver's output pulls down with 4A current for 80ns initially and then folds back to 3 Ohm holding low, which provide necessary damping to the gate loop oscillation. To adjust MOSFET's switching speed, the driver provides a driving current programming pin to facilitate circuit tuning. The driver is the industry's first SiC MOSFET driver IC, integrating negative bias and active Miller effect suppression function and eliminating gate resistors. It provides a convenient, compact and reliable gate drive solution for SiC MOSFETs. The driver is suitable for Si MOSFET and IGBT drive as well.

Device Information

PART NUMBER	PACKAGE	PACKING
IVCR1412SR	SOT-23-6	Tape and Reel

Typical Application Diagram



Pin Layout

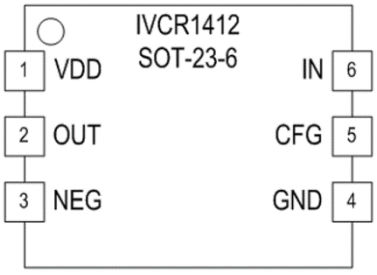


Table of Contents

4. Pin Configuration and Functions

PIN	NAME	I/O	DESCRIPTION
1	VDD	P	Positive power supply
2	OUT	O	Driver output before a negative voltage capacitor
3	NEG	O	Driver negative output, connecting to negative voltage capacitor and MOSFET Gate
4	GND	G	Driver ground
5	CFG	I	Output turn-on current configuration input
6	IN	I	Driver input

5. Specifications

5.1 Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Total supply voltage	-0.3	30	V
OUT	Gate driver output voltage	-0.3	V_{DD}+0.3	V
IN	Signal input voltage	-5	30	V
CFG	Configuration input voltage	-0.3	5.5	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2 ESD Rating

		Value	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operation Conditions

		MIN	MAX	UNIT
V_{DD}	Total supply voltage	4.5	25	V
V_{IN}	Driver input voltage	0	25	V
T_A	Operating ambient temperature	-40	125	°C

5.4 Electrical Specifications

Unless otherwise noted, V_{DD} = 15 V, T_A = –40°C to 125°C
Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{DDq}	Quiescent current	IN=0V		0.7		mA
UVLO						
V_{ON}	Under voltage lockout thresholds	Rising threshold		4.1	4.4	V
V_{OFF}		Falling threshold	3.5	3.7		V
INPUT (IN)						
V_{INH}	Input rising threshold			1.9	2.2	V
V_{INL}	Input falling threshold		1	1.2		V
V_{INHYS}	Input hysteresis			0.7		V
V_{INNS}	Input negative voltage		-5			V
Configuration (CFG)						
V_{CFG}	CFG voltage			1.2		V
Output						
I_{OH}	Peak source current	C_{LOAD} =0.22uF, R_{CFG}=NC		2		A
		C_{LOAD} =0.22uF, R_{CFG}=16kOhm		1.55		
		C_{LOAD} =0.22uF, R_{CFG}=5kOhm		1.2		
		C_{LOAD} =0.22uF, R_{CFG}=64kOhm		0.9		
I_{OLF}	Peak pulse sink current	C_{LOAD} =0.22uF		4		A
T_{OLF}	Peak sink current pulse width			80		ns
V_{OH}	Output high voltage	I_{OUTH} = -10mA, R_{CFG}=NC		VDD-0.02	0.035	V
		I_{OUTH} = -10mA, R_{CFG}=16kOhm		VDD-0.0225		
		I_{OUTH} = -10mA, R_{CFG}=5kOhm		VDD-0.03		
		I_{OUTH} = -10mA, R_{CFG}=64kOhm		VDD-0.04		
V_{OL}	Output low voltage	I_{OUTL} = 10mA		0.02	0.038	V
R_{OH}	Output pull-up resistance	R_{CFG}=NC		2	3.5	Ω
		R_{CFG}=16kOhm		2.6		
		R_{CFG}=5kOhm		3.3		
		R_{CFG}=64kOhm		4.4		
R_{OL}	Output pull-down resistance after T_{OLF}			2	3.8	Ω
V_{NEG}	NEG negative voltage	OUT=L		-2		V
Timing						
TD_{RR}	Rising delay	C_{LOAD} = 1.8nF, R_{CFG}=NC		15	30	ns
TD_{FF}	Falling delay			15	30	ns
T_R	Rise time			12	30	ns
T_F	Fall time			6	12	ns

6. Typical Characteristics

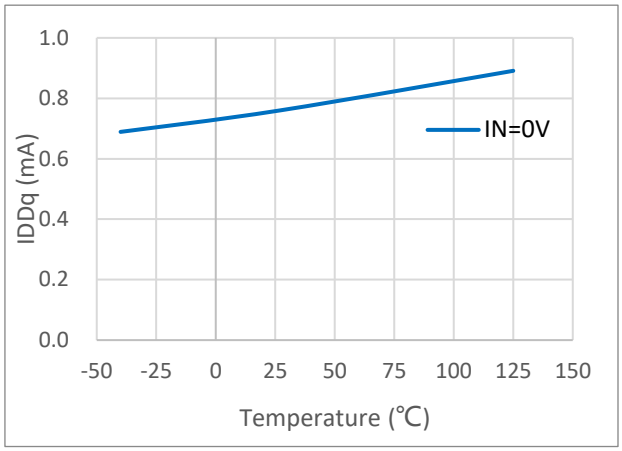


Figure 1. IDDq vs Temp

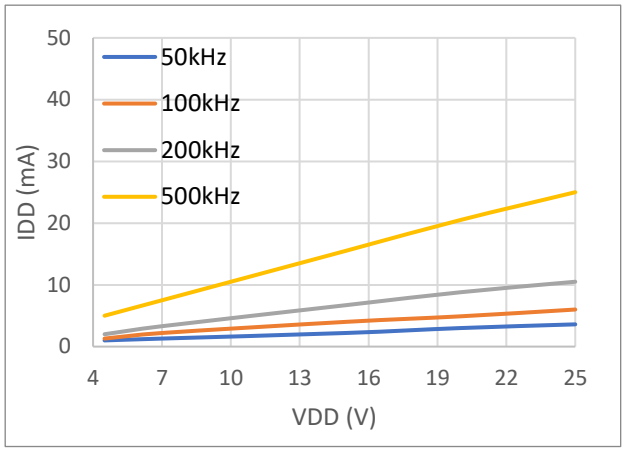


Figure 2. IDDq vs VDD

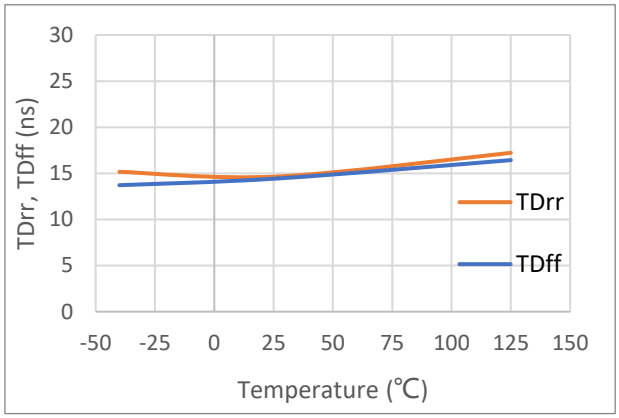


Figure 3. TDrr、TDff vs Temp

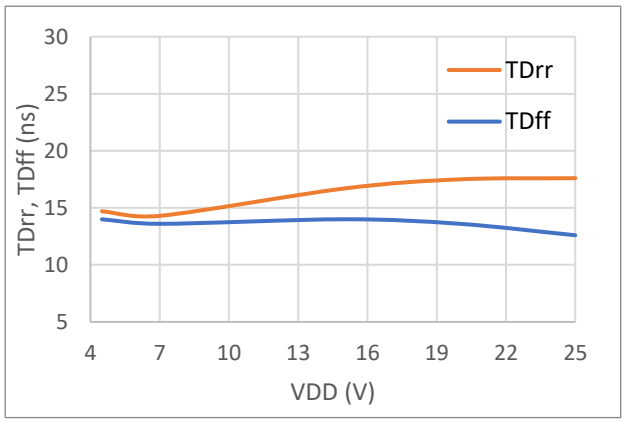


Figure 4. TDrr、TDff vs VDD

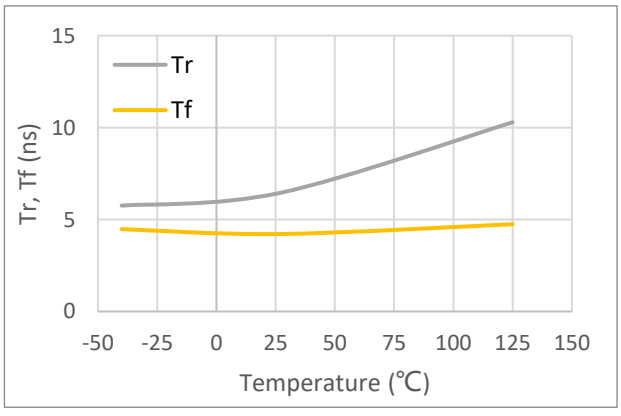


Figure 5. Tr、Tf vs Temp

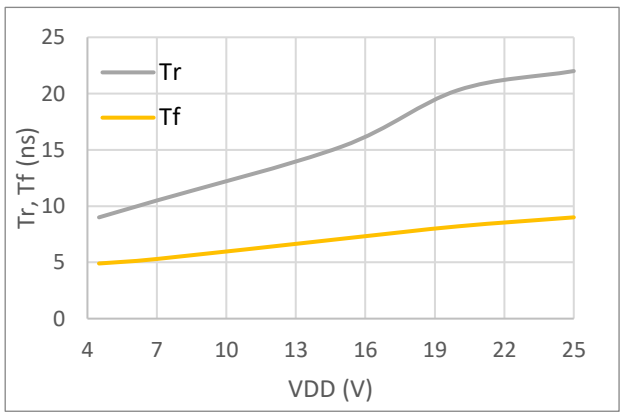


Figure 6. Tr、Tf vs VDD

7. Detail Descriptions

IVCR1412 is a compact SiC MOSFET driver providing single-channel high-speed low-side gate drive. With configurable sourcing current, it eliminates output gate resistors and minimizes gate drive loop stray inductance. It features negative bias output and active Miller clamp, which improves driver noise immunity when SiC MOSFETs are switching.

7.1 IN

IN is a non-inverting logic gate driver input. The input pin has a weak pull-down. When left floating, the output is pulled to GND. The input is compatible to TTL and CMOS logic levels with maximum 30V voltage tolerance.

7.2 OUT

OUT is the gate driver output. OUT consists of a configurable pullup and fixed pulldown output stage. It can supply up to 2A peak source and 4A peak sink current pulses. OUT swings between VDD and GND providing rail-to-rail operation. The peak 4A sink current lasts for 80ns. After the 80ns timer expires, OUT is held low by a 3 Ohm pull-down resistance, which provides damping to the gate driver loop. The presence of the driver output MOSFET body diodes also offers voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

7.3 VDD and Under Voltage Lock-Out

IVCR1412 absolute maximum voltage rating is 30V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The driver has internal under voltage lockout (UVLO) protection feature. When VDD level is below UVLO threshold, this circuit holds the output LOW, regardless of the status of the input.

7.4 CFG

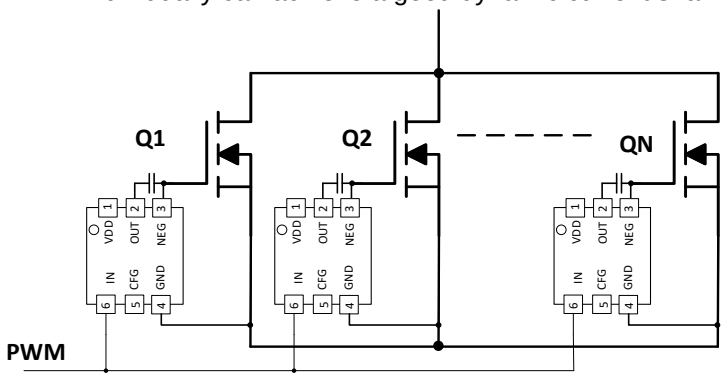
CFG is an output sourcing current programming pin. It provides 4-step sourcing current programming, from 0.9A to 2A. Output sinking current is fixed. Leaving CFG pin open will set the output sourcing current to its maximum 2A value.

7.5 NEG

NEG is the output capacitor charging and voltage regulation pin. It regulates the capacitor voltage to maintain -2V between NEG and OUT pins. If the negative turn-off voltage is desired, NEG should be connected to MOSFET gate directly which swings between VDD-2V and -2V. If 0V turn-off voltage is preferred, OUT should be connected to MOSFET gate. To reduce charge sharing effect, the negative voltage capacitor between NEG and OUT should be at least 10x larger than MOSFET gate capacitance. 1uF capacitance is recommended.

8. Application and Implementation

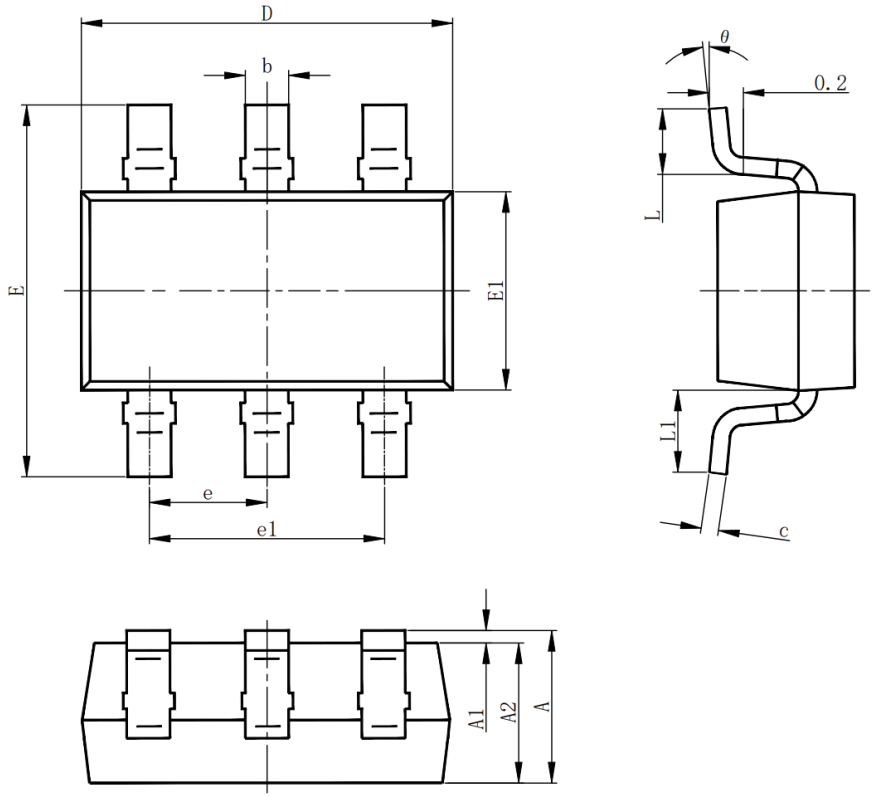
To achieve dynamic current sharing of paralleled MOSFETs at turn-on and turn-off edges, gate resistors are often used to decouple the MOSFET gates from each other. However, the inserted gate resistors and any resistance in a gate drive loop would reduce the circuit's driving strength against Miller effect. By using current source drive and Miller clamp, IVCR1412 effectively eliminates gate resistors and offers a simple way to counteract Miller effect. Due to the short propagation delay and minimum device to device mismatch, paralleled MOSFETs driven by IVCR1412 individually can achieve a good dynamic current sharing.



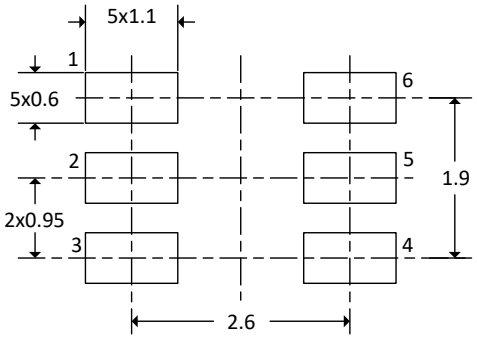
Paralleled MOSFETs' driving circuit for dynamic current sharing

9. Package Information

SOT-23-6 Package Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.600REF.		0.024REF.	
θ	0°	8°	0°	8°



SOT-23-6 Recommended Soldering Dimensions